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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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MORGAN LEWIS & BOCKIUS LLP
1111 PENNSYLVANIA AVENUE NW
WASHINGTON, DC 20004

EXAMINER	
DI GRAZIO, JEANNE A	
ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 11/05/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/893,991	Applicant(s) CHUNG ET AL.	
	Examiner Jeanne A. Di Grazio	Art Unit 2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 August 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Priority

Priority to Korean Patent Application No. 2000-38015 (July 4, 2000) is claimed.

Response to Arguments

As an initial matter, the Examiner thanks Applicant's representative for having taken the time for an interview on July 31, 2003.

Upon further search, however, the Examiner has discovered new prior art of record and rejects all claims as follows.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4 rejected under 35 U.S.C. 102(b) as being anticipated by Atherton (US 6,078,364).

Per claim 1 (amended): Atherton discloses the conventional elements of a first substrate and a second substrate coupled to the first substrate with a liquid crystal layer interposed between the first and second substrates (Col. 1, Lines 15-19). Though not clearly illustrated in Figure 2, Atherton has a plurality of select lines (Applicant's scan lines 32) and a plurality of data lines (38) arranged over the first substrate, the scan lines (select lines 32) must intersect the data lines to define pixel areas (Figure 2, pixel areas 30), thin film transistors (MOS transistors 40) over the first substrate adjacent intersections of the scan and data lines, pixel electrodes

respectively arranged in corresponding pixel areas such that each pixel electrode is substantially bilaterally symmetric about a vertical reference line crossing the center of the respective corresponding pixel area in a direction of the data lines (the pixel of Figure 2 is the same on both sides with reference to the data lines (38)).

Per claim 2: Each of the pixel electrodes has a shape in which a lower right corner and a lower left corner thereof are removed (Figure 2).

Per claim 3: Each of the pixel electrodes has a lower center projection extending downwardly (Figure 2).

Per claim 4: Each of the pixel electrodes is electrically connected to a TFT at the lower center projection thereof (Figure 4).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5-9 rejected under 35 U.S.C. 103(a) as being unpatentable over Atherton (US 6,078,364) in view of Yamamoto et al. (US 6,088,071).

Per claims 5-9: Atherton discloses pixel areas (Figure 2, pixel areas 30) including a pixel electrode, a pair of a first projection and a second projection projecting from an adjacent select line (Applicant's scan line, 32) at one side, the first projection being separated from the second projection, a thin film transistor (TFT, MOS 40) formed adjacent an intersection of the adjacent scan (select) line and an adjacent data line. As noted, Atherton has a pixel electrode with a

projection connected to the TFT and the projection of the pixel electrode being disposed between first and second projections of the adjacent scan line (Figure 2). The pixel electrode furthermore has a shape avoiding the first and second projection (Figure 2). The pixel is also substantially bilaterally symmetric (Figure 2).

Atherton does not appear to explicitly disclose a storage capacitor electrode connected to the pixel electrode, the storage capacitor including an electrode overlapping with the second projection of the scan line for an adjacent pixel area.

However, Yamamoto discloses an auxiliary (storage capacitor) connected to a pixel electrode (Figure 1, auxiliary electrode 30 and pixel electrode 19), the storage capacitor including an electrode overlapping with a projection of a gate (Applicant's scan) line for an adjacent pixel area (Figure 1, gate line projection 15b). Furthermore, a portion of the pixel is removed to accommodate a capacitance (Figure 1)(Col. 6, Lines 18-30). That a storage capacitor includes an electrode overlapping with either first or second projections of a scan line results in functional equivalents of each other.

Yamamoto has this arrangement (the arrangement of Figure 1) for high aperture ratio and improved quality of display (Col. 6, Lines 18-30).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Atherton in view of Yamamoto for high aperture ratio and thus improved quality of display as taught in Yamamoto.

Claims 10-12 rejected under 35 U.S.C. 103(a) as being unpatentable over Atherton (US 6,078,364) in view of Yamashita et al. (US 5,659,375).

Per claims 10-12: In Figure 2, Atherton discloses a base plate (Applicant's substrate, 26), a plurality of select lines (Applicant's scan lines 32) over the substrate, extending substantially in a horizontal direction (extends in rows); a plurality of data lines (38) over the substrate, extending substantially in a vertical direction (extends in columns) to intersect the scan (select) lines, the select (scan) lines and the data lines defining an array of pixel areas (30) over the substrate; a thin film transistor (MOS 40) in each pixel area, one terminal of the thin film transistor being connected to one of the adjacent select (scan) lines (Col. 3, Lines 20-38); and a pixel electrode in each pixel area (Col. 3, Lines 1-19), connected to still another terminal of the thin film transistor in the pixel area (Col. 3, Lines 35-36).

In Figure 2, the pattern of the pixel electrode is symmetric about a virtual line extending substantially vertically and passing a center of the pixel area (Figure 2).

The pixel electrode has a substantially rectangular pattern in which a lower right corner and a lower left corner thereof are removed by substantially the same amount (Figure 2).

Atherton does not appear to explicitly specify that the pixel electrode has a pattern configured to yield substantially the same capacitance value for capacitors that are formed between the pixel electrode and adjacent data line on one side and between the pixel electrode and the adjacent data line on another side.

However, Yamashita discloses:

"[EXAMPLE 1]- FIG. 1 is a plan view of a first example of an active matrix substrate according to the present invention. One of a plurality of identical pixel sections of the substrate is shown here. In the figure, the same reference numerals as those used in FIG. 5 designate the same parts as those of the conventional active matrix substrate 201.

In the active matrix substrate 101, the pixel electrode 14 is formed with portions thereof overlaid on the data signal lines 11a and 11b on both sides thereof, with an interlevel insulating film interposed to prevent the pixel electrode 14 from short-circuiting to the data signal lines 11a and 11b. In forming the pixel electrode 14, the area of the portion overlapping the data signal line 11a and the area of the portion overlapping the data signal line 11b are adjusted **so that the coupling capacitance C.sub.SD1 in FIG. 7, i.e., the capacitance between the pixel electrode and the data signal line 11a, becomes approximately equal to the coupling capacitance C.sub.SD2 in FIG. 7, i.e., the coupling capacitance between the pixel electrode and the data signal line 11b.**

In the liquid crystal display panel of the present example, the liquid crystals are driven by the data signal having polarity which is inverted between fields or between frames and is inverted from one data signal line to the next, that is, from the data signal line 11a to the data signal line 11b.

Next, the effect and advantage of the above structure will be described. In the active matrix substrate 101, since the pixel electrode 14 is formed overlapping the data signal lines 11a and 11b on both sides thereof and sandwiching an interlevel insulating film therebetween, the direction of the field electric being applied to the liquid crystals near the periphery of the pixel electrode 14 is prevented from being disturbed by the potentials of its adjacent data signal lines.

Furthermore, since the coupling capacitances 35 and 36 between the pixel electrodes 14 and the data signal lines 11a and 11b on both sides thereof are approximately equal, the variation of the pixel potential through the coupling capacitances from the adjacent data signal lines can be cancelled out. Accordingly, in the driving method involving inverting the data signal polarity between fields or between frames, the occurrence of crosstalk in vertical directions can be eliminated by making provisions so that data signals of different polarities are applied to the data signal line 11a and data signal line 11b, respectively.

Thus, the present example eliminates the occurrence of crosstalk in vertical directions while at the same time preventing the disruption of the liquid crystal orientation caused by electric field disturbances from the data

signal lines on both sides of the pixel electrode." (Col. 6, Lines 66-67 and Col. 7, Lines 1-41).

Yamashita has the above structure to eliminate crosstalk in vertical directions while at the same time preventing disruption of the liquid crystal orientation caused by electric field disturbance from the data signal lines on both sides of the pixel electrode (Col. 7, Lines 36-41).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Atherton in view of Yamashita to eliminate crosstalk in vertical directions while at the same time preventing disruption of the liquid crystal orientation caused by electric field disturbance from the data signal lines on both sides of the pixel electrode (Col. 7, Lines 36-41).

Claims 13-20 rejected under 35 U.S.C. 103(a) as being unpatentable over Atherton (US 6,078,364) in view of Yamashita et al. (US 5,659,375) and further in view of Yamamoto et al. (US 6,088,071).

Per claims 13-20: Atherton does not appear to explicitly specify each pixel area including a storage capacitor connected to the pixel electrode for the pixel area, and wherein an area occupied by the storage capacitor for a pixel area extends into an adjacent pixel area; however, Yamamoto has an auxiliary electrode (Figure 1, auxiliary electrode 30) connected to the pixel electrode for the pixel area (pixel 19) and an area occupied by the storage capacitor for a pixel area extends into an adjacent pixel area (Figure 14 and Col. 6, Lines 18-30). Yamamoto has this configuration for improved aperture ratio (Id.). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Atherton in view of Yamamoto for improved aperture ratio.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeanne A. Di Grazio whose telephone number is (703)305-7009. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Kim, can be reached on (703) 305-3492. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Jeanne Andrea Di Grazio

JDG

Robert Kim, SPE

T. Chowdhury
Primary Examiner